DEPARTMENT OF COMPUTER ENGINEERING

GOVERNMENT ENGINEERING COLLEGE DAHOD

GUJARAT TECHNOLOGICAL UNIVERSITY

Semester 4

Term: Even 2017-18 [26th Dec 2017 – 20th April 2018]

COMPUTER ORGANIZATION [2140707]

ALA topics for presentation with scheduled date

Note:

1. Students should only present ppt after approval by faculty (V J Patel).
2. PPT should be shown for correction during TUTORIAL presentation.
3. Every time PPT should be sent to faculty through email only.
4. Subject of email id should be ALA [subjectcode_enrollment] ex. ALA 2140707_110180107001
5. Name of PPT should be subjectcode_enrollment.pptx ex. 2140707_110180107001_110180107002.pptx

#	Group Name	Topic	Date of Presentation
1	MAHIMA-RABAB	Cache Memory (Chapter 4 from COA book by William Stallings)	Will be updated Soon
2	NIKUL-MEET	Integer Representation and Integer Arithmetic (Chapter 9 from COA book by William Stallings)	"
3	MOHAMD-ALI	Floating Point Representation and Floating Point Arithmetic (Chapter 9 by William Stallings)	"
4	RIDDHI-AVANI	Instruction Cycle and Instruction Pipelining	"
5	ANUJA-DIMPLE	Programmed I/O and Interrupt Driven I/O (Refer any reference book)	"
6	AKSHAY-UTTAM	Booths Multiplication Algorithm	"
7	HARPREET-DAINISHA	DMA (Refer all reference books)	"
8	KAJAL-ANJALI	Asynchronous Data Transfer	"
9	KASHYAP-AHMED	Instruction Pipelining	"
10	YASH-TAHER	Types of Operations done by Instruction Sets (10.4 Stallings)	"
11	NIMISHA-AVLIKA	The Stack and Data Storage (4.1 COA, Alan Clements)	"
12	AMIT-RAVI	Data Processing and Data Movement (4.4 COA, Alan Clements)	"
13	TAHER-KALIM	Memory Indirect Addressing (4.5 COA, Alan Clements)	"
14	ANSHU-NIKHIL	Branch Prediction, Static and Dynamic Branch Predictions (7.5 COA, Alan Clements)	"
15	ANUJ-NIKUNJ	Introduction to Pipelining (7.3 COA, Alan Clements)	"
16	MARUT-DHARMESH	Introduction to Cache Memory (9.1 COA, Alan Clements)	"

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17	SHUBHAM-DEVID	Virtual Memory and Memory Management (9.5 COA, Alan Clements)	“
18	RAJ	Bus Clocking, Bus Arbitration and Bus Operations (3.4.4/5/6, Section 3.4, Tanenbaum)	“
19	JAY-RUDRA	Out-Of-Order Execution and Register Renaming (4.5.3, Section 4.5, Tanenbaum)	“
20	PARTH-SANJAY	Expanding Opcodes (5.3.2, Section 5.3, Tanenbaum)	“
21	NIKHIL-YOGESH	Traps and Interrupts (5.6.4 and 5.6.5, Tanenbaum)	“
22	HARSHNA-NISHA	Implementation of Segmentation (6.1.7, Tanenbaum)	“
23	HARSHITA	Demand Paging and the Working Set Model (6.1.3, Tanenbaum)	“
24	JAYKUNJ-NIKUNJ	The assembly process, Linking and Loading (7.3, 7.4, Tanenbaum)	“
25	DHRUV-MANISH	The Microarchitecture Level (Chapter 4, Tanenbaum)	“
26	AHMED-SAHIL	Virtual Memory Organization (Refer all reference books)	“